AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A spilt gate flash memory cell structure ~~for prevention reverse tunneling~~ comprising:

a semiconductor region within a substrate extending to a surface;

a gate insulator layer formed over said semiconductor surface;

a conductive floating gate disposed over said gate insulator layer;

a floating gate insulator layer disposed over said floating gate; [[and]]

sidewall insulator spacers disposed along bottom portions of sidewalls of said floating gate on ~~adjacent to~~ said gate insulator layer ~~,where etching processes used to fashion said sidewall insulator spacers from a spacer insulator layer, etch said spacer insulator layer faster than said gate insulator layer and said floating gate insulator layer~~;

an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate insulator layer and said sidewall insulator spacers; and

a conductive control gate disposed over said intergate insulator layer and covering a portion ~~about half~~ of said floating gate.

2. (Original) The structure of Claim 1 wherein said semiconductor region is a silicon region.

3. (Original) The structure of Claim 1 wherein said substrate is a silicon containing substrate.

4. (Original) The structure of Claim 1 wherein said gate insulator layer is a thermally grown oxide layer grown to a thickness of about 50 to 200 angstroms.

5. (Original) The structure of Claim 1 wherein said conductive floating gate is composed of polysilicon.

6. (Original) The structure of Claim 1 wherein said floating gate insulator layer is a grown polysilicon oxide layer grown to a thickness of about 800 to 2000 Angstroms.

7. (Original) The structure of Claim 1 wherein said spacer insulator is an oxide layer.

8. (Original) The structure of Claim 1 wherein said spacer insulator layer is a PECVD oxide layer.

9. (Original) The structure of Claim 1 wherein said spacer insulator layer is a deposited oxide layer, said gate insulator layer is a thermal oxide layer and said floating gate insulator layer is a polysilicon oxide layer.

10. (Canceled)

11. (Original) The structure of Claim 1 wherein said intergate insulator layer is an oxide layer.

12. (Original) The structure of Claim 1 wherein said conductive control gate is composed of polysilicon.

13. – 27. (Canceled)

28. (New) A spilt gate flash memory cell structure comprising:

a semiconductor region within a substrate extending to a surface;

a gate insulator layer formed over said semiconductor surface;

a conductive floating gate disposed over said gate insulator layer, the gate insulator layer extending outside of the conductive floating gate;

a floating gate insulator layer disposed over said floating gate;

sidewall insulator spacers disposed along bottom portions of sidewalls of said floating gate adjacent said gate insulator layer;

an intergate insulator layer disposed over exposed portions of said gate insulator layer, said floating gate insulator layer and said sidewall insulator spacers; and

a conductive control gate disposed over said intergate insulator layer and covering a portion of said floating gate.